ABSTRACT OF THE DISCLOSURE

This semiconductor device comprises: a first signal path for guiding the input signal from a first pad to the input terminal of the macro cell; a second signal path for guiding the clock from a second pad to the clock input terminal of the macro cell; a third signal path for guiding a output signal from the signal output terminal of the macro cell to a third pad; and a forth signal path for receiving the clock from the first signal path and guiding the clock to a fourth pad. It is possible to eliminate the wiring delay by measuring the time from when the input signal and clock are supplied by the first and second pad until the output signal is output by the third pad, and the time from when the clock is supplied to the second path until it is output by the fourth pad.